

WHAT IS CLAIMED IS:

1 1. A trace buffer circuit comprising:
2 a plurality of interconnected registers, including a
3 first end register to input and output instruction addresses,
4 a second end register, and a plurality of middle registers
5 connected between said first end register and said second end
6 register; and

7 a write path to shift an instruction address in one
8 of said plurality of interconnected registers by two registers
9 toward the second end register on a write operation.

1 2. The circuit of claim 1, further comprising:
2 a read path to shift the instruction address by one
3 register toward the first end register on a read operation.

1 3. The circuit of claim 1, wherein the trace buffer
2 operates as a first-in first-out (FIFO) register on the write
3 operation and a last-in first-out (LIFO) register on the read
4 operation.

1 4. The circuit of claim 1, wherein the instruction
2 address comprises a 32-bit word.

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5. The circuit of claim 4, wherein each of the first and second end registers and the plurality of interconnected registers comprise a 32-bit register.

6. The circuit of claim 5, wherein the plurality of interconnected registers comprise thirty-two registers.

7. The circuit of claim 5, further comprising:
a 64-bit write bus to write a 64-bit address pair to the first end register and an adjacent register on the write operation; and

a 32-bit read bus to read a 32-bit instruction address from the first end register on the read operation.

8. The circuit of claim 1, further comprising:
a first holding register;
a second holding register;
a first comparator to compare a new branch target

address in the first holding register to a stored branch target address in the first end register;

a second comparator to compare a new branch source address in the second holding register to a stored branch source address in a first adjacent register, said first adjacent register being connected to the first end register on the read path; and

12 a compression indication circuit to generate a
13 compression indicator in response to the new branch target
14 address matching the stored branch target address and the new
15 branch source address matching the stored branch source
16 address.

1 9. The circuit of claim 8, wherein the compression
2 indication circuit operates to set a least significant bit of
3 the stored branch target address in response to the new branch
4 target address matching the stored branch target address and
5 the new branch source address matching the stored branch
6 source address.

1 10. The circuit of claim 8, further comprising:
2 a second adjacent register in said plurality of
3 registers, said second adjacent register being connected to
4 the first adjacent register on the read path;
5 a third adjacent register in said plurality of
6 registers, said third adjacent register being connected to the
7 second adjacent register on the read path;
8 a third comparator to compare a new branch target
9 address in the first holding register to a stored branch
10 target address in the second adjacent register; and

11 a fourth comparator to compare a new branch source
 12 address in the second holding register to a stored branch
 13 source address in the third adjacent register,
 14 wherein the compression indication circuit operates
 15 to generate a compression indicator in response to the new
 16 branch target address matching the stored branch target
 17 address in the second adjacent register and the new branch
 18 source address matching the stored branch source address in
 19 the third adjacent register.

1 11. The circuit of claim 10, wherein the compression
 2 indication circuit operates to set a least significant bit of
 3 the stored branch source address in the third adjacent
 4 register in response to the new branch target address matching
 5 the stored branch target address in the second adjacent
 6 register and the new branch source address matching the stored
 7 branch source address in the third adjacent register.

1 12. The circuit of claim 1, further comprising a valid
 2 bit buffer comprising:
 3 a first end flip-flop to input and output valid bits
 4 from the valid bit buffer;
 5 a second end flip-flop;

a plurality of interconnected flip-flops connected between said first end flip-flop and said second end flip-flop;

a write path to shift a valid bit in one of said plurality of interconnected flip-flops by two flip-flops to a downstream flip-flop on a write operation; and

a read path to shift the valid bit by one flip-flop toward an upstream flip-flop on a read operation.

13. A pipelined processor comprising:

a trace buffer circuit connected to the pipelined digital signal processor, said trace buffer circuit comprising:

a plurality of interconnected registers, including a first end register to input and output instruction addresses, a second end register, and a plurality of middle registers connected between said first end register and said second end register;

a write path to shift an instruction address in one of said plurality of interconnected registers by two registers toward the second end register on a write operation; and

a read path to shift the instruction address by one register toward the first end register on a read operation.

14. The processor of claim 13, wherein the trace buffer operates as a first-in first-out (FIFO) register on the write operation and a last-in first-out (LIFO) register on the read operation.

15. The processor of claim 13, wherein the instruction address comprises a 32-bit word.

16. The processor of claim 15, wherein each of the first and second end registers and the plurality of interconnected registers comprise a 32-bit register.

17. The processor of claim 16, further comprising:
a 64-bit write bus to write a 64-bit address pair to the first end register and an adjacent register on the write operation; and
a 32-bit read bus to read a 32-bit instruction address from the end first register on the read operation.

1 18. A method for compression, comprising:
 2 setting a least significant bit of a branch target
 3 address in the stored address pair in response to a new
 4 address pair matching a stored address pair.

1 19. The method of claim 18, further comprising:
 2 discarding the new address pair in response to the
 3 new address pair matching the stored address pair.

1 20. The method of claim 18, further comprising:
 2 storing the stored address pair in a first pair of
 3 registers; and
 4 comparing the new address pair to the stored address
 5 pair.

1 21. The method of claim 20, further comprising:
 2 writing the new address pair to the first pair of
 3 registers in response to the new address pair not matching the
 4 stored pair.

1 22. The method of claim 20, further comprising:
 2 comparing the new address pair to a second stored
 3 address pair in a second pair of registers adjacent the first
 4 pair of registers;

5 setting a least significant bit of a branch source
6 address in the second stored address pair in response to the
7 new address pair matching the second stored pair; and

8 writing the new address pair to the first pair of
9 registers in response to the new address pair not matching the
10 second stored pair.

1 23. The method of claim 22, further comprising:

2 discarding the new address pair in response to the
3 new address pair matching the second stored address pair.

1 24. A method for tracing instructions executed by a
2 processor, comprising:

3 writing a $2n$ -bit address pair in a first-in first-
4 out write operation; and

5 reading an n -bit address in a last-in first-out read
6 operation.

1 25. The method of claim 24, wherein n is thirty-two.

1 26. The method of claim 24, wherein the address pair
2 comprises a branch target address and a branch source address.

1 27. An apparatus, including instructions residing on a
2 machine-readable medium, for use in a trace buffer, the
3 instructions causing the machine to:

4 set a least significant bit of a branch target
5 address in a stored address pair in response to a new address
6 pair matching the stored address pair.

1 28. The apparatus of claim 27, further comprising
2 instructions causing the machine to:
3 discard the new address pair in response to the new
4 address pair matching the stored address pair.

1 29. The apparatus of claim 27, further comprising
2 instructions causing the machine to:
3 store the stored address pair in a first pair of
4 registers; and
5 compare a new address pair to a stored address pair
6 in the first pair of registers.

1 30. The apparatus of claim 29, further comprising
2 instructions causing the machine to:
3 write the new address pair to the first pair of
4 registers in response to the new address pair not matching the
5 stored pair.

1 31. The apparatus of claim 29, further comprising
2 instructions causing the machine to:

3 compare the new address pair to a second stored
4 address pair in a second pair of registers adjacent the first
5 pair of registers;

6 set a least significant bit of a branch source
7 address in the second stored address pair in response to the
8 new address pair matching the second stored pair; and

9 write the new address pair to the first pair of
10 registers in response to the new address pair not matching the
11 second stored pair.

1 32. The apparatus of claim 31, further comprising
2 instructions causing the machine to:

3 discard the new address pair in response to the new
4 address pair matching the second stored address pair.